CLAIMS

We claim:

1. A method of operating a programmable logic device comprising:

applying a full supply voltage to operate one or more active blocks of the programmable logic device; and

applying a reduced supply voltage to operate one or more inactive blocks of the programmable logic device.

2. The method of Claim 1, wherein the step of applying a full supply voltage comprises:

applying a first supply voltage to a first source/drain of an n-channel transistor;

applying a boosted voltage, greater than the first supply voltage, to a gate of the n-channel transistor; and

applying the full supply voltage at a second source/drain region of the n-channel transistor.

3. The method of Claim 2, wherein the boosted voltage is approximately 2 to 2.5 times greater than the first supply voltage.

4. The method of Claim 1, wherein the step of applying a reduced supply voltage comprises:

applying a first supply voltage to a first source/drain of an n-channel transistor;

applying a standby voltage, less than the first supply voltage, to a gate of the n-channel transistor; and

applying the reduced supply voltage at a second source/drain region of the n-channel transistor.

5. The method of Claim 4, further comprising controlling the standby voltage such that the reduced supply voltage is about half of the first supply voltage.

6. The method of Claim 3, wherein the standby voltage is approximately 80 to 100 percent of the first supply voltage.

7. The method of Claim 1, wherein the step of applying the reduced supply voltage is performed in response to user controlled signals.

8. The method of Claim 7, further comprising defining the user controlled signals during run time of the programmable logic device.

9. The method of Claim 7, further comprising generating the user controlled signals in response to operating conditions of the programmable logic device during run time.

10. The method of Claim 1, wherein the step of applying the reduced supply voltage is performed in response to configuration data bits stored by the programmable logic device.

11. The method of Claim 10, further comprising defining the configuration data bits during design time of the programmable logic device.

12. The method of Claim 1, further comprising selecting the reduced supply voltage to be a minimum voltage required to retain data stored in the one or more inactive blocks.

13. A programmable logic device comprising:

a first voltage supply terminal configured to receive a first supply voltage;

a plurality of programmable logic blocks; and

a plurality of high voltage transistors, wherein each of the transistors has a gate, a first source/drain region coupled to the first voltage supply terminal, and a second source/drain region coupled to a corresponding one of the programmable logic blocks; and

a plurality of control circuits, each configured to provide a control voltage to the gate of a corresponding one of the high voltage transistors.

14. The programmable logic device of Claim 13, further comprising a plurality of user control terminals, each configured to provide a corresponding user control signal to a corresponding one of the control circuits.

15. The programmable logic device of Claim 14, wherein each control circuit provides the control voltage in response to the corresponding user control signal.

16. The programmable logic device of Claim 13, further comprising a plurality of configuration memory cells, each configured to provide a corresponding configuration data bit to a corresponding one of the control circuits.

17. The programmable logic device of Claim 16, wherein each control circuit provides the control voltage in response to the corresponding configuration data bit.

18. The programmable logic device of Claim 13, further comprising a plurality of feedback lines, each coupling the second source/drain region of each of the plurality of high voltage transistors to a corresponding control circuit.

19. The programmable logic device of Claim 13, wherein the plurality of high voltage transistors comprise a plurality of n-channel transistors.

20. The programmable logic device of Claim 19, wherein each of the plurality of high voltage transistors has a gate dielectric layer that is about 4 to 6 times thicker than gate dielectric layers present in the plurality of programmable logic blocks.